Amendments to the Specification:

Please replace the paragraph, beginning at page 3, line 1, with the following rewritten paragraph:

Fig. 4 is a diagram showing a case where the capacitor unit is formed by series-parallel connection, in which N capacitors are interconnected in series-parallel where ~~M series~~ P series are interconnected, in accordance with the exemplary embodiment.

Please replace the paragraph, beginning at page 3, line 19, with the following rewritten paragraph:

Fig. 2 is a diagram explaining the voltage on the high potential side of the capacitor unit in accordance with the exemplary embodiment of the present invention. In capacitor unit 7 of Fig. 2, N capacitors 71, 72, 73 ... 7N are interconnected in series, and the both ends thereof are connected to output terminal 110 and ground terminal 120, respectively. The example where all of capacitors 71 through 7N are interconnected in series is described hereinafter, but they may be interconnected in series-parallel. The N is called series number. In other words, only series connection is employed as in Fig. 2, the number of capacitors is equivalent to series number N. Fig. 4 is a diagram showing a case where a capacitor unit of the exemplary embodiment of the present invention is formed by series-parallel connection, in which N capacitors are interconnected in series-parallel where ~~M series~~P series are interconnected in parallel. Assuming N is 4 and ~~M is 3~~P is 3, for example in Fig. 4, four capacitors are interconnected in series and three series of capacitors are interconnected in parallel, thereby forming a capacitor unit in a matrix shape. In this case, series number N is 4.